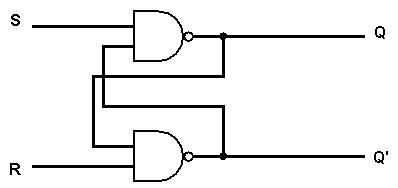
**CS1026 Hilary Term Lab 3**

**Aim**: To design a gated S-R flip-flop (latch) circuit with the following properties:

* Allows inputs to affect the outputs only when C=1
* When C=0, the latch holds the last state value at its output

An S-R latch circuit is a bistable multivibrator, which means it has two stable states. A simple S-R latch circuit has only two inputs (set and reset) and two outputs (Q and Q’) which should always be compliments of eachother (an invalid input of 11 causes Q=Q’=0).

The simple S-R latch is shown below:



A *gated* S-R latch is a circuit which adds extra logic gates (and inputs) to add extra logical conditions, ie: only being able to change state when C=1.

From the definition of the gated S-R latch that we want to design, we can determine its truth table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| C | S | R | Q | Q’ |
| 0 | 0 | 0 | *Latch* | *Latch* |
| 0 | 0 | 1 | *latch* | *latch* |
| 0 | 1 | 0 | *Latch* | *Latch* |
| 0 | 1 | 1 | *Latch* | *Latch* |
| 1 | 0 | 0 | *Latch* | *latch* |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |

The term *latch* denotes that the output is determined by previous inputs.

From the truth table of the simple S-R latch, we can see that the latch state is achieved when both the set and reset inputs of the latch circuit are 0. We want to design the circuit so that this is the case when C is 0, and that the circuit operates as a latch when C is 1.

This is represented algebraically below:

Where is the function we need, and X represents the inputs to the latch circuit (S,R).

Clearly the logical operation/ gate we want to employ is AND.

With the above reasoning, we can now construct the required gated S-R latch circuit:

